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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,313	01/22/2002	Yasuaki Hirano	204552022200	4784

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EXAMINER	
HO, HOAI V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/051,313	Applicant(s) HIRANO, YASUAKI
	Examiner Hoai V. Ho	Art Unit 2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

1. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) was considered.

Papers submitted under 35 U.S.C. 119(a)-(d) have been placed of record in the file.

2. Claims 1-12 are presented for examination.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the **external power source** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-10 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In claim 1, line 20 an "external power source", in claim 7, "wherein an output voltage of the external power source during erasure is a voltage higher than the erase voltage" and in claim 9, "wherein the voltage of the external power source during erasure is 9 V or higher" are not described in the specification.

Claims 2, 5 and 6 are rejected for incorporating the defects of the parent claim.

Claims 3, 4, 8, and 10 are rejected due to the rejections of the parent claim.

6. Claims 2, 4, 6, 8 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2, lines 3 and 4, a "voltage boosting circuit provided between the external power source and the resistance element" is unclear and confusing. How does it relate to a "resistance element inserted between the regulator circuit and an external power source" in lines 19 and 20 of claim 1? And how does the external power source relate to the voltage boosting circuit?

Claim 6 is rejected for incorporating the defects of the parent claim.

Claims 4 and 8 are rejected due to the rejections of the parent claim.

For the purpose of rejection, an "external power supply Vcc or Vpp" is used for an "external power source" in lines 19 and 20 of claim 1 or in line 4 of claim 4, respectively.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-6, 8, 10, 11 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Ninomiya USP 5617359.

As per claim 1, Figure 3 of Ninomiya is directed to a nonvolatile semiconductor memory device, comprising: a plurality of floating gate field effect transistors (M11-Mmn) each having a control gate, a floating gate, a drain and a source and capable of electrically writing and erasing

data, the floating gate field effect transistors being arrayed in a matrix on a substrate or a well; a plurality of row lines each connected to control gates of the floating gate field effect transistors arrayed in a row direction; a plurality of column lines each connected to drains of the floating gate field effect transistors arrayed in a column direction (col. 5, lines 9-42); a common source line (Vs) connected to sources of the floating gate field effect transistors constituting a block; a regulator circuit (15) for supplying a voltage applied to the common source line at least during erasure (col. 7, lines 7-14); a resistance element (25a of fig. 9) inserted between the regulator circuit and an external power source (Vcc through the boost circuit Vpp); voltage level detecting means (15d) for instructing start of the erase voltage application to the common source line, detecting that an input voltage from the resistance element to the regulator circuit reaches a prescribed voltage level and instructing termination of the erase voltage application to the common source line (ST11 of fig. 6); and erase voltage applying means (Qp3) for receiving an instruction from the voltage level detecting means and applying an erase voltage from the regulator circuit to the common source line (col. 7, line 64 to col. 8, line 50).

As per claims 2-6, Ninomiya, starting column 7, lines 64-64 and column 11, lines 25- further comprising: a voltage boosting circuit provided between the external power source and the resistance element, wherein an output voltage from the voltage boosting circuit is supplied to the regulator circuit via the resistance element.

As per claims 8 and 10, Ninomiya, starting at column 7, lines 36-38 and lines 64-66 discloses wherein an output voltage of the voltage boosting circuit during erasure is a voltage higher than the erase voltage.

As per claims 11 and 12 (method), they encompass the same scope of invention as to that of claims 1 and 2 (apparatus claims) except they draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

9. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Ema (5274599) discloses a nonvolatile memory device having precise erasing levels.

10. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

11. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (703) 308-4839. Other inquiries of this application should be called to (703) 308-0956 or the fax number (703) 308-7722.

H. Ho
March 6, 2003

Hoai V. Ho
Primary Examiner
Art Unit 2818